FPGA Timeline & Applications
FPGAs past, present & future

Jim Brakefield

FPGA Application Areas

$6-7B yearly sales

- Communications
- DSP
- Software-defined radio
- Aerospace and defense systems
- ASIC prototyping
- Medical imaging
- Computer vision
- Speech recognition
- Cryptography
- Bioinformatics
- Computer hardware emulation
- Data Center: AI, NN, big data

Advantages:
Low NRE
Low volume products
Updates/patches
Parallelism
Portable code (RTL)
Soft dev || Hard dev
Early use of process nodes

Disadvantages:
ASICs are cheaper,
faster and lower power
in high volumes

Low End Applications

1.5-3mm pkg, 2K LUTs
.1Mb block RAM

- Glue logic

    Connection of disparate devices to a uP

    Last minute patches

20K LUTs, 40 DSPs,
1Mb block RAM

- Logic funnel

    Legacy design re-hosting

    IP: pre-packaged modules

    Soft core processors & peripherals (www.opencores.org)

Mid-scale Applications

200K LUTs, 1K DSPs, 15Mb block RAM

- Communications: Internet routers, Telephone switches, Protocol conversion
- Signal Processing: Software defined radio, Camera, Audio, Video, Radar …
- Test & Measurement: high speed A2D & D2A,
- Big science: Super-collider, SETI, etc.
- Aerospace: radiation hardened, military temperature range
- SOC (System On a Chip): driverless vehicles

High End Applications

2.5M LUTs, 5K DSPs,
200Mb block RAM

- ASIC (Applications Specific Integrated Circuit) emulation

- High end weapons, who knows what else?

- Super-computing coprocessor

    Intel bought Altera

- Wall street (high frequency trading)

- AI/deep NN/data center acceleration

The Vendors

- Xilinx: www.xilinx.com
  - Originated FPGAs, tried anti-fuse, flash & CPLD, now #1
- Altera (now Intel):   www.altera.com
  - Originally CPLDs, currently #2 in FPGAs.
- Microsemi (was Actel): www.actel.com
  - Originally anti-fuse, then flash, now SRAM & flash based
- Lattice Semiconductor: www.latticesemi.com
  - Offer tiny FPGA chips, diversifying away from FPGAs
- uP with some programmable logic
  - Cypress (under PSoC): ARM + programmable IO
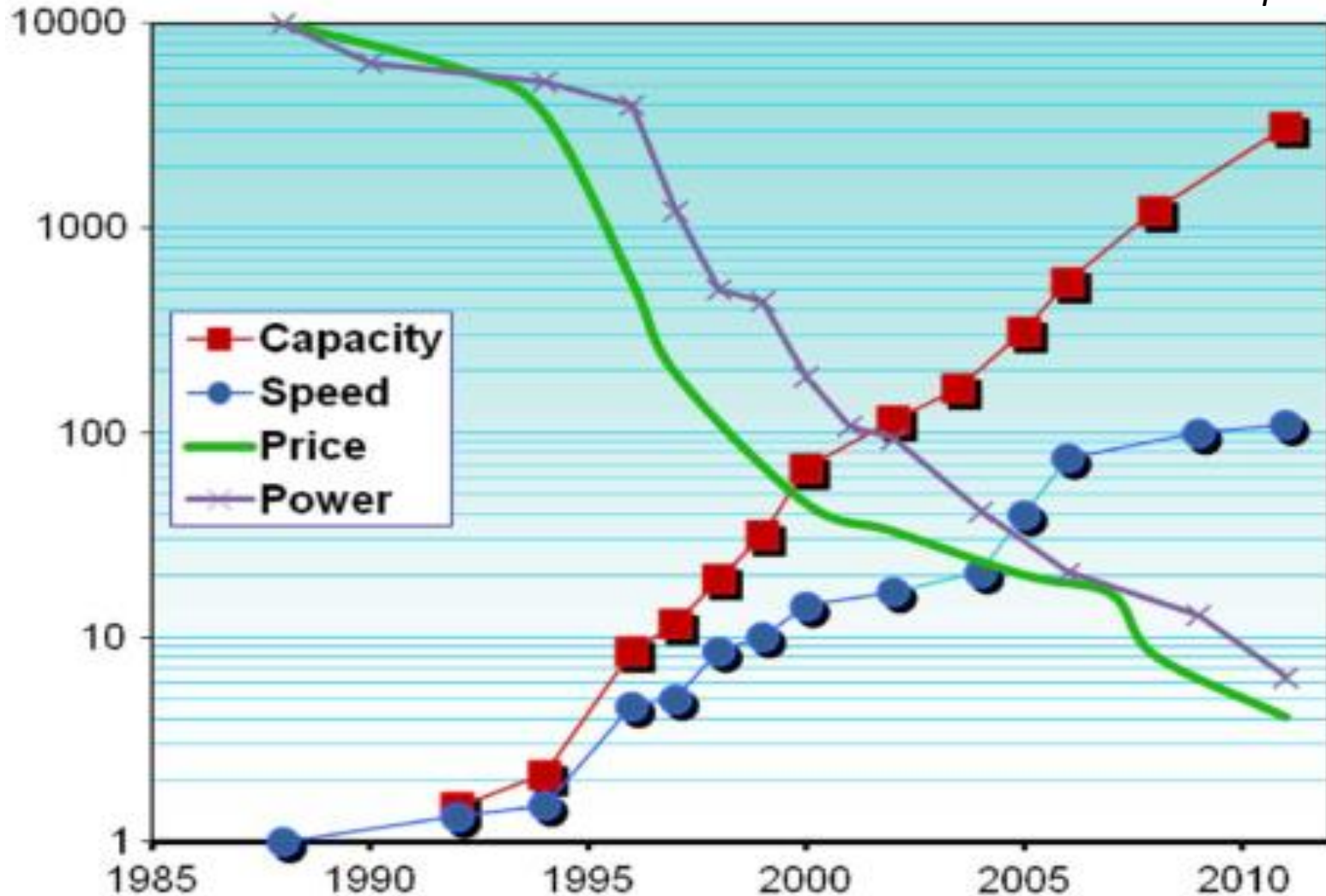 - Atmel/Microchip: ibid.

The FPGA
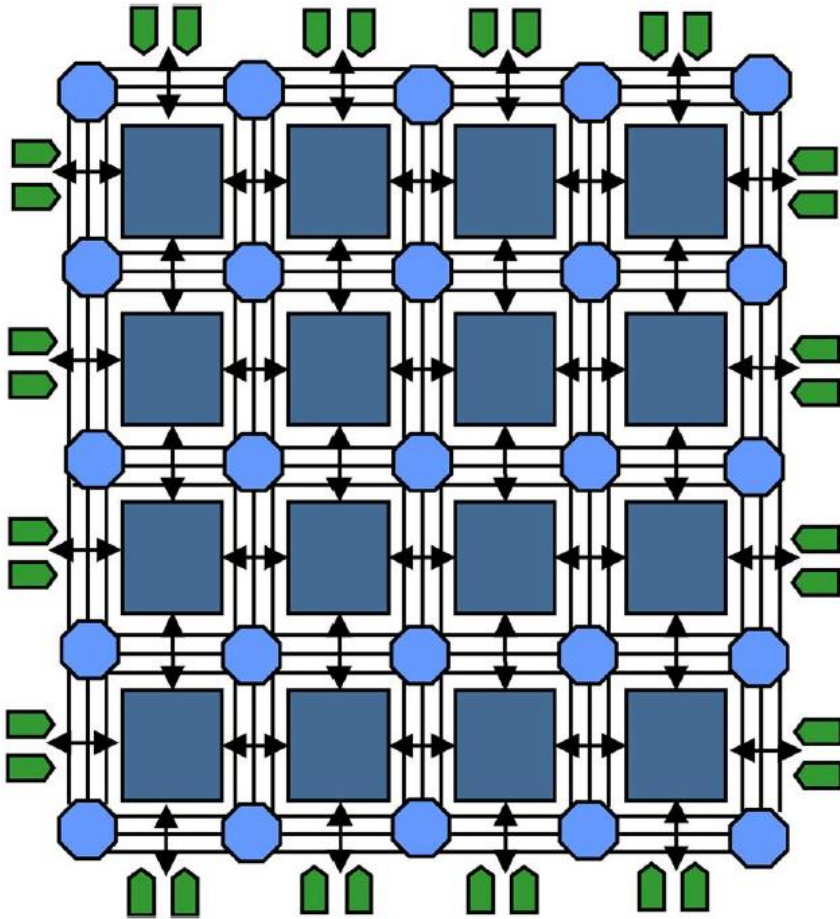
Generic FPGA diagram
Green: IOs
Squares: LUT
  groups/slices/blocks
Octagons: Wiring
 interconnections
Lines: Wire
  segment bundles

From: Trimberger, 2015 Proc IEEE v103 #03 pg320
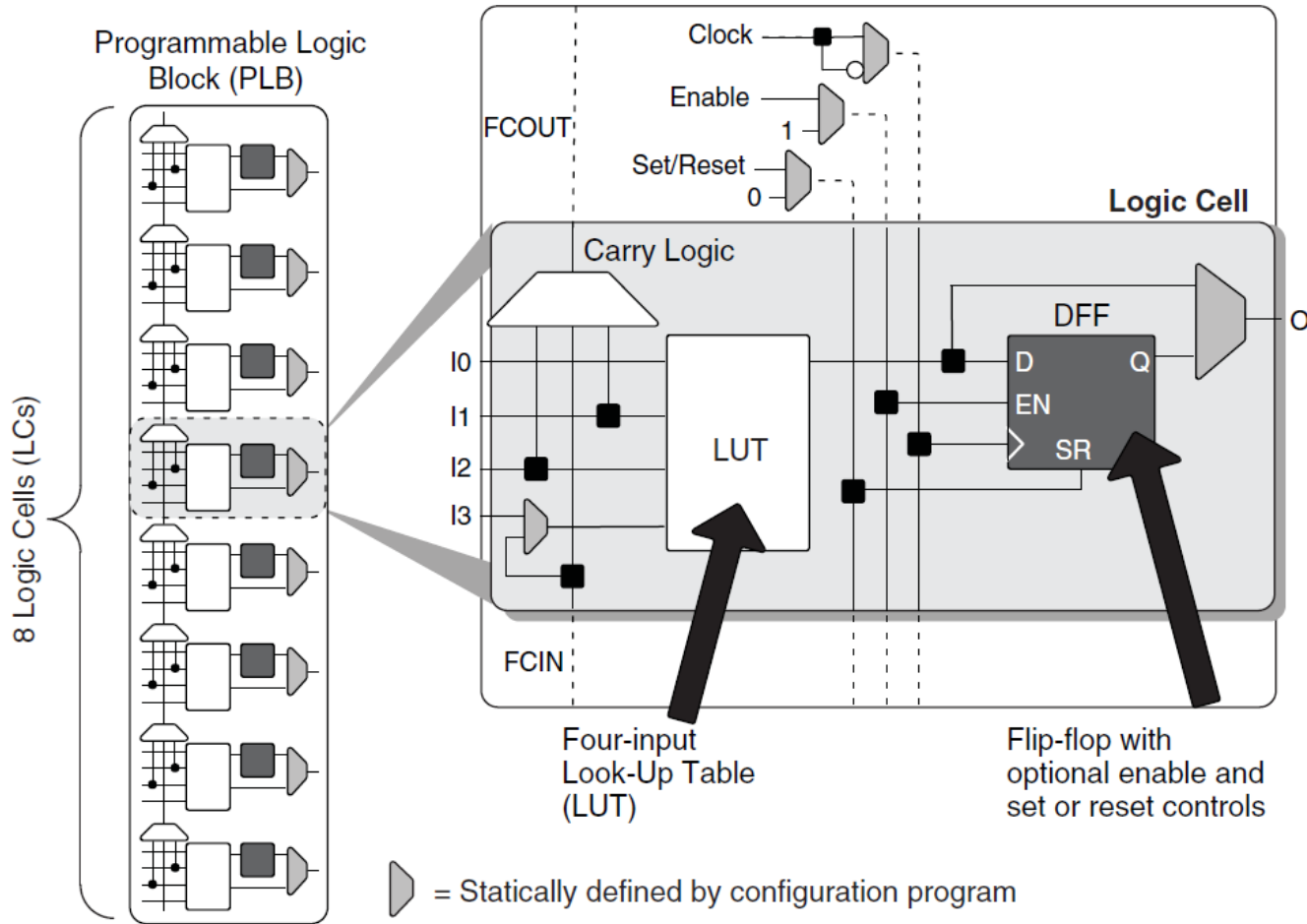
FPGA timeline

From: Trimberger, 2015 Proc IEEE v103 #03 pg318

Basic LUT (Look-Up Table)

Currently up to 2.5M LUTs at 100-1000 LUTs/$

- 1985   LUTs plus DFF   Xilinx XC2000
  - Clocking facilities
  - Configuration memory
  - Routing wires
- 1991   Carry chain   Xilinx XC4000
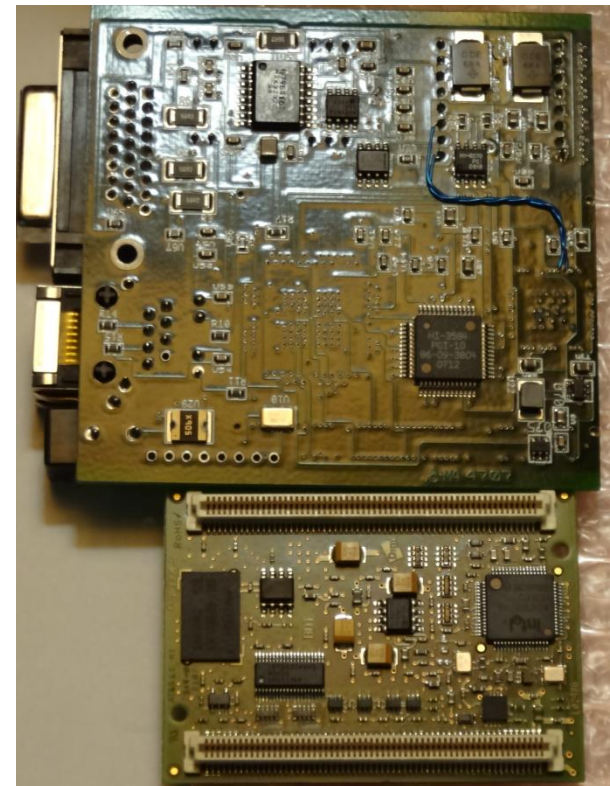 - LUT RAM (16x1)
  - Shift Registers

LUT + DFF

3LUTs tried
6LUTs in use
ALM: ~two
  5LUTs
  with
  multiple
  configurations

Programmable Logic
Block (PLB)

8 Logic Cells (LCs)

Clock

Enable
                1
FCOUT
Set/Reset
                0

Logic Cell

Carry Logic

DFF

I0   D   Q   O
I1   EN
          LUT
I2   >   SR
I3

FCIN

Four-input
Look-Up Table
(LUT)

Flip-flop with
optional enable and
set or reset controls

4LUT: 16 bits
of memory &
a 16:1 MUX

⊳ = Statically defined by configuration program

Lattice Semiconductor iCE40FamilyHandbook.pdf pg6-2

Uses:

"glue" logic
Reprogrammable
(field changes)
Reliability
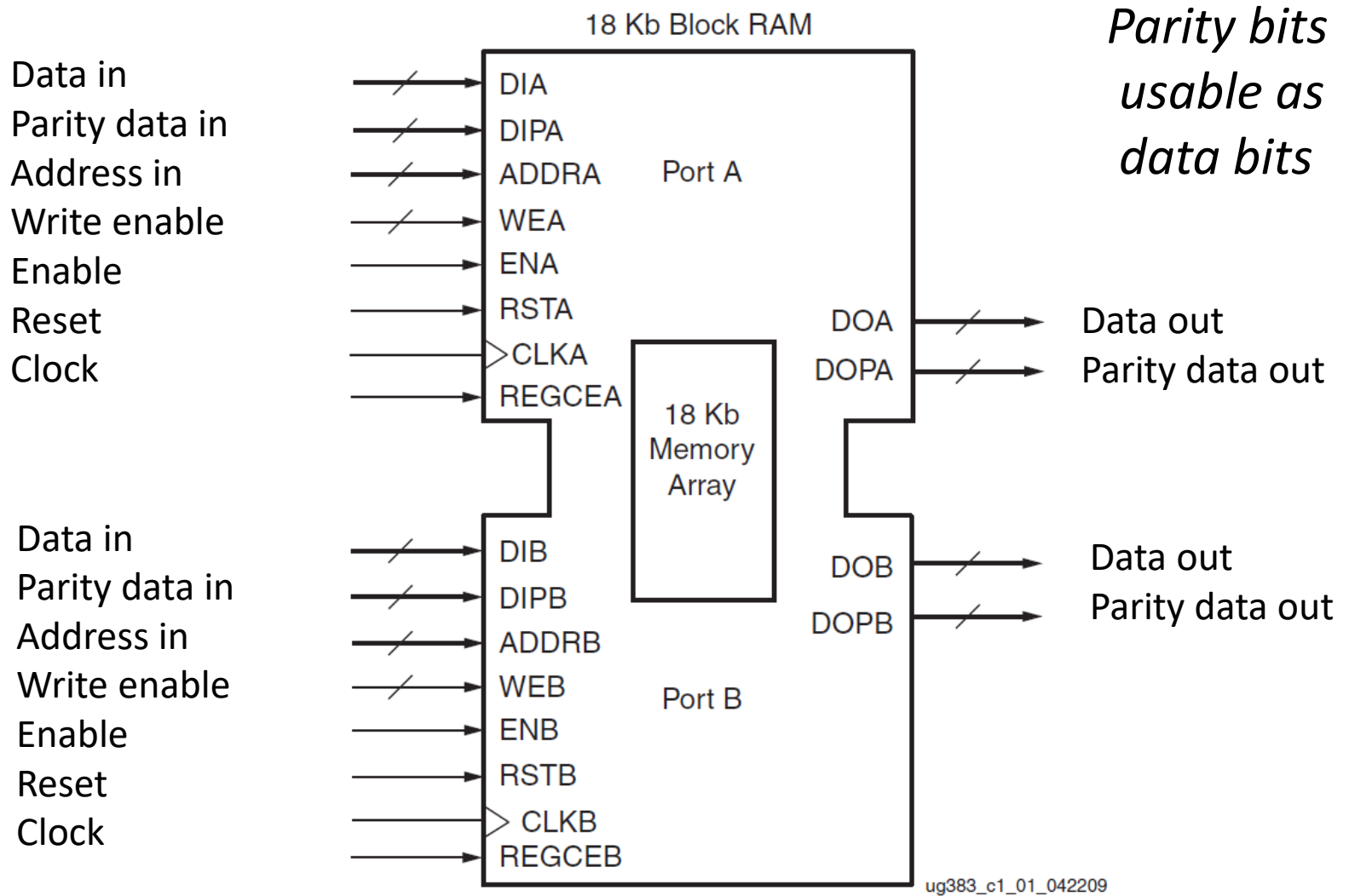*(parts count and*
wiring reduction)
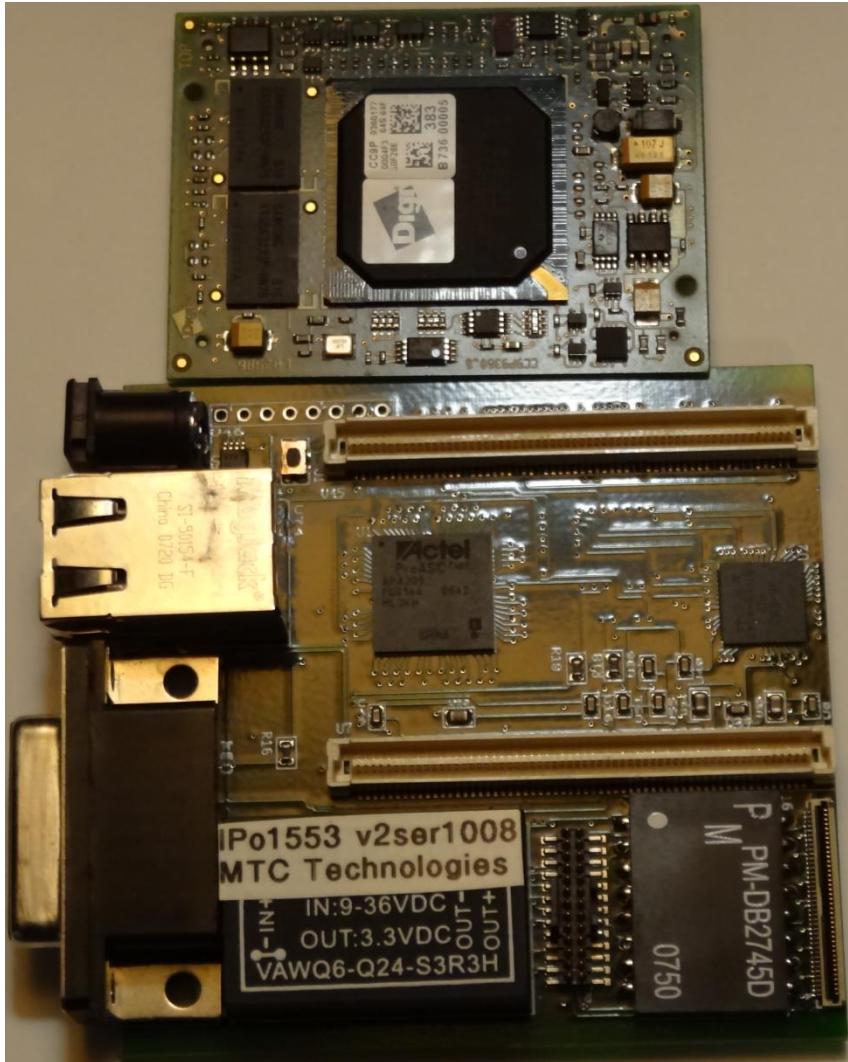
IPo1553 module (BAE Systems): ARINC 429, MIL-STD 1553, RJ45, CAN

Block RAM

up to ~12K block RAMs
up to 480M bits

- 1995   Dual port RAM   Altera FLEX
-       Variable aspect ratio (on each port)

  16Kx1, 8Kx2, 4Kx4, 2Kx8/9, 1Kx16/18, 512x32/36

-               A variety of RAM capacities

  LUT RAM (16x1), small block RAM (~32x18), block RAM (~512x36), large block RAM (~4Kx72)

-                Uses:

  Buffers, FIFOs, shift registers, scratch pad memory, DSP coefficients, two single port RAMs, u-code

Block RAM

18 Kb Block RAM

Parity bits usable as data bits

Data in	→	DIA
Parity data in	→	DIPA
Address in	→	ADDRA
Write enable	→	WEA
Enable	→	ENA
Reset	→	RSTA
Clock	→	CLKA
	→	REGCEA

Port A

18 Kb Memory Array

DOA → Data out
DOPA → Parity data out

Data in	→	DIB
Parity data in	→	DIPB
Address in	→	ADDRB
Write enable	→	WEB
Enable	→	ENB
Reset	→	RSTB
Clock	→	CLKB
	→	REGCEB

Port B

DOB → Data out
DOPB → Parity data out

ug383_c1_01_042209

Xilinx Spartan-6 FPGA Block RAM Resources User Guide pg12

PLL (Phase Locked Loop)

FPGA internal clocks to 800MHz

- 1996   Altera FLEX 10K

- FPGAs can have dozens of distinct clocks

- All the analog (of the PLL) inside FPGA

- Uses: Reduce chip count, precise clock phase control

"ASIC" IO

- 1998   Universal IO   Xilinx Virtex
- 1.2, 1.8, 2.5, 3.3, 5.0 VDC
    each bank of IO pins has its own power supply
- LVTTL, CMOS, HSTL, SSTL, PECL, LVDM …
    (via constraint file)
- 4, 8, 12, 16, 24ma, pullup/pulldown (ibid)
- resistive termination, slow/fast edges (ibid)
- Uses:
  general purpose IO, DRAM hookup, PWM, logic analyzer, etc.

"ASIC" IO

Up to 1680 IOs/chip

Global input buffers used for clocks and reset

To Device Pin

Lattice Semiconductor iCE40FamilyHandbook.pdf pg6-7
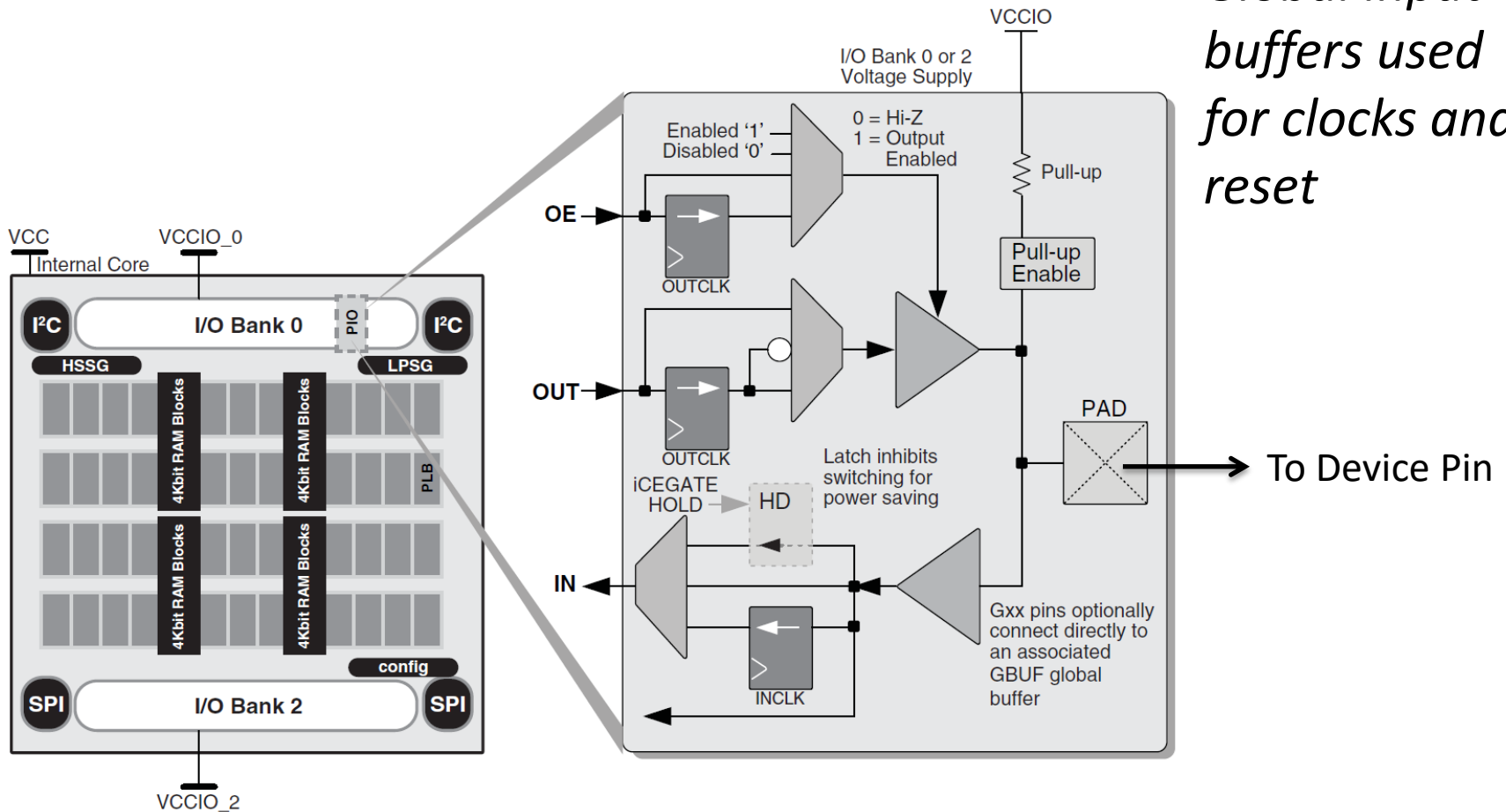
Multiply/accumulator

up to ~12K per chip running at 800MHz

- 2000   18x18 signed   Xilinx Virtex-2

- 2002   DSP block   Altera Stratix

- Initially no accumulator, accumulators now include ALU capability and floating-point

- Use pipelining for maximum speed

- Multiplier shapes: 16x16, 18x18, 18x27; (3)9x9, (2)18x18 or (1)27x27

- Uses: DSP, FFT, ALU

Simplified DSP slice

Xilinx Spartan-6 FPGA DSP48A1 Slice pg 17
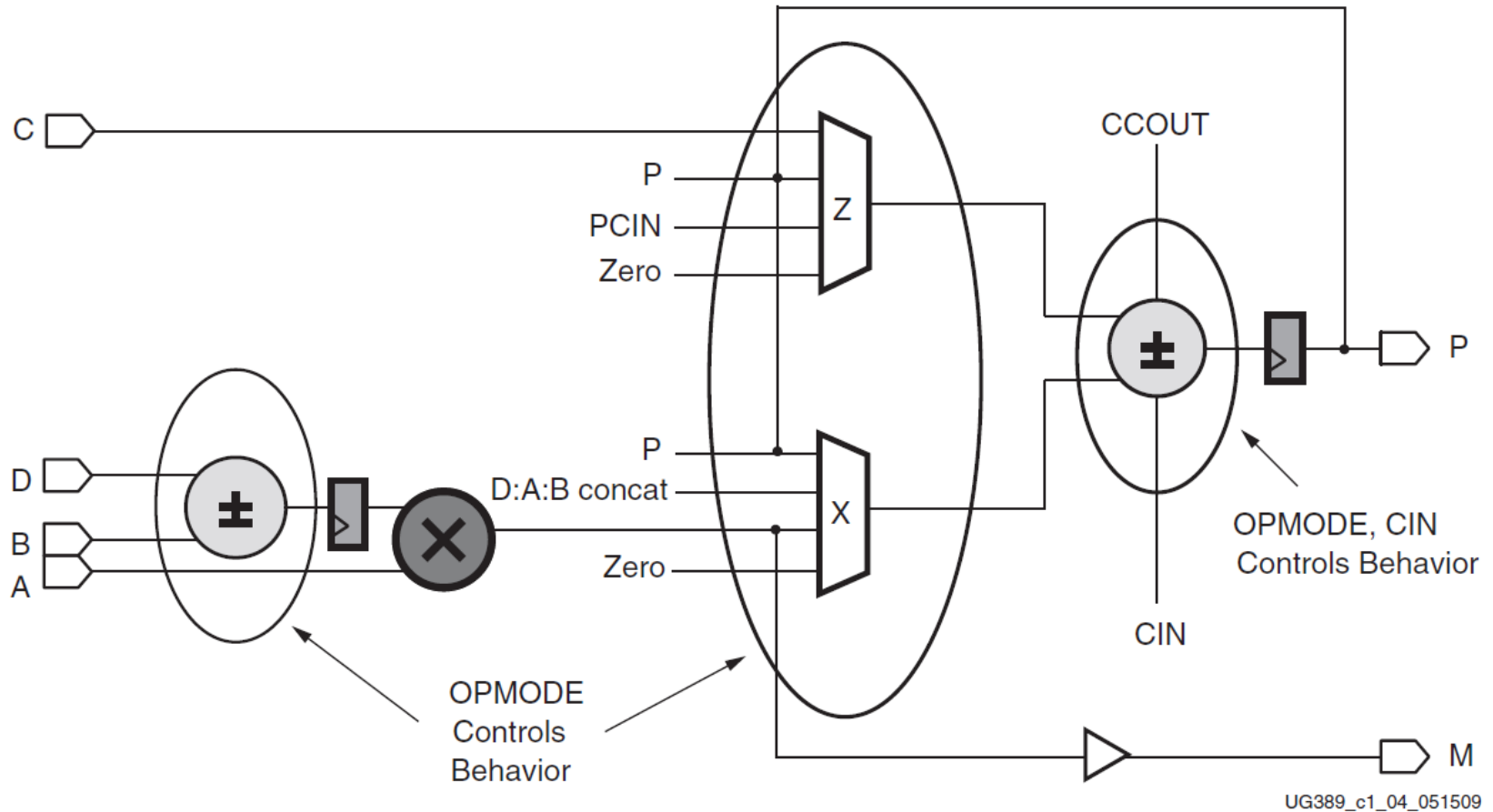
SERDES (Serialize/De-serialize)

up to ~100 per chip
up to 56Gbps

- 2001   Source synchronous transceiver
       Xilinx Virtex-II

- 2002   SERDES Transceiver

      Xilinx Virtex-II Pro

- Uses:

   Communication links: Fiber connections, Ethernet, PCI-express, Interlaken, etc

ASIC micro-processor(s)

*1 to 6 per chip, 100MHz to 1.5GHz*

- 2000   ARM 9   Altera Excalibur
- 2002   PowerPC   Xilinx Virtex-II Pro
- 2010   ARM Cortex M3   Actel Smart Fusion
- 2010   ARM dual Cortex A9
                        Xilinx Zynq, Altera Cyclone V
- 2015   ARM quad A53 & dual R5, GPU
                        Xilinx Zynq Ultrascale+, Altera Arria-10
- 2019   ACAP   Xilinx datacenter compute chip
- 2019   ?   Intel/Altera ?
- All have microprocessor peripherals
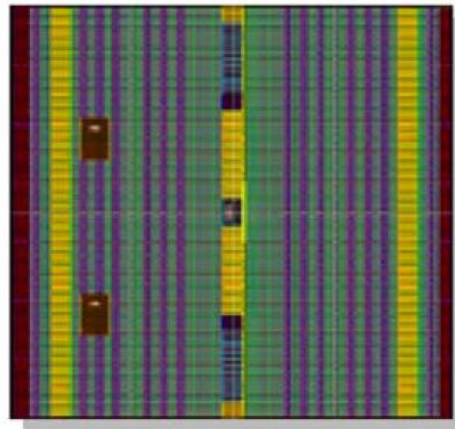- Uses: Reduce chip count, cleaner interface between uP and FPGA fabric

SOC chip

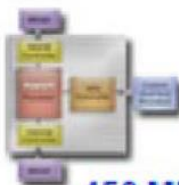**Virtex-4: A "Platform FPGA"**

200,000 Flexible Logic Cells
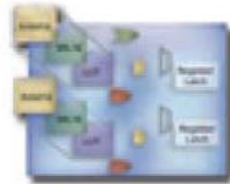
500 MHz Digital Clock Management

500 MHz, 10Mbits BRAM with FIFO & ECC

0.6-11.1 Gbps Serial Transceivers — 11.1 Gbps

AES Design Encryption

450 MHz PowerPC® Processor with Auxiliary Processing Unit 10/100/1000 Ethernet MAC

500 MHz Programmable DSP Execution Units

1 Gbps Source Synchronous I/O

From: Trimberger, 2015 Proc IEEE v103 #03 pg327

Zynq: ARM + FPGA chip

HC23.18.322.Zynq-7000-EPP-Dutta_Xilinxrevised.pdf
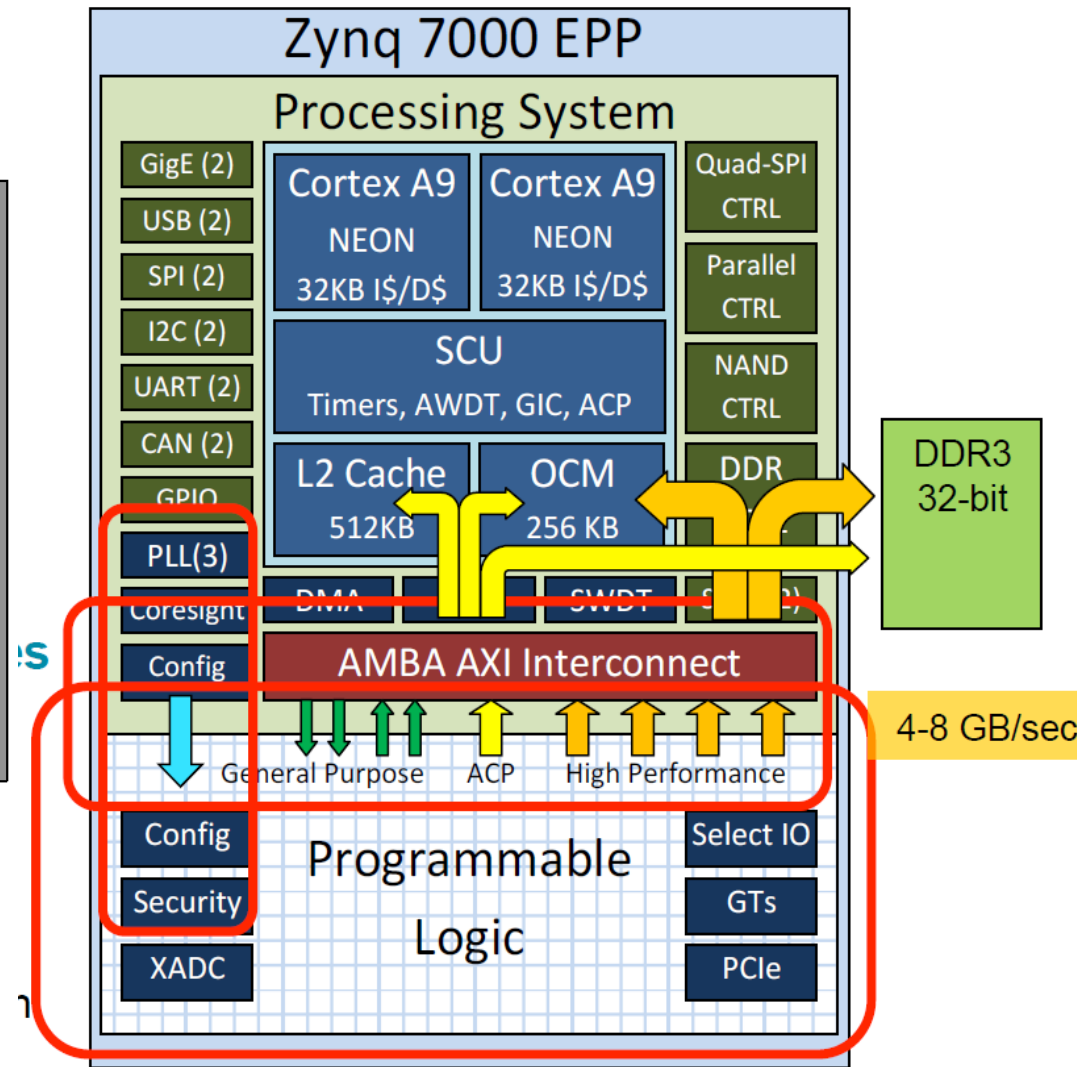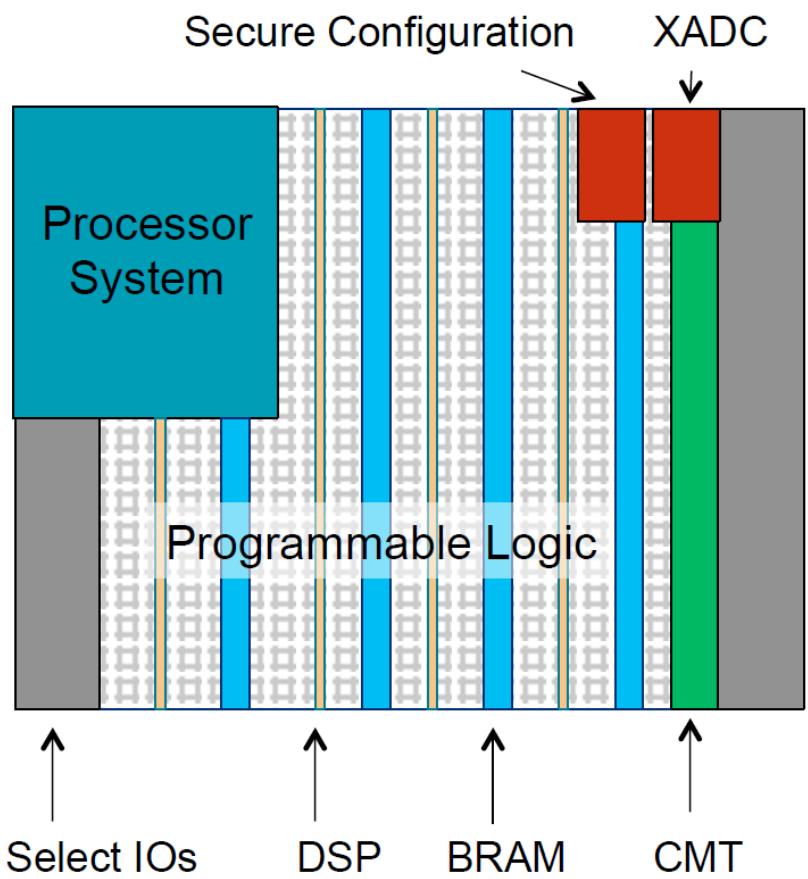
Silicon interposer (3D silicon)

- 2009   Multi-chip FPGA   Xilinx Virtex-6

Uses: Yield improvement, reduced wiring capacitance, augmentation with SERDES, DRAM & A2D/D2A chips
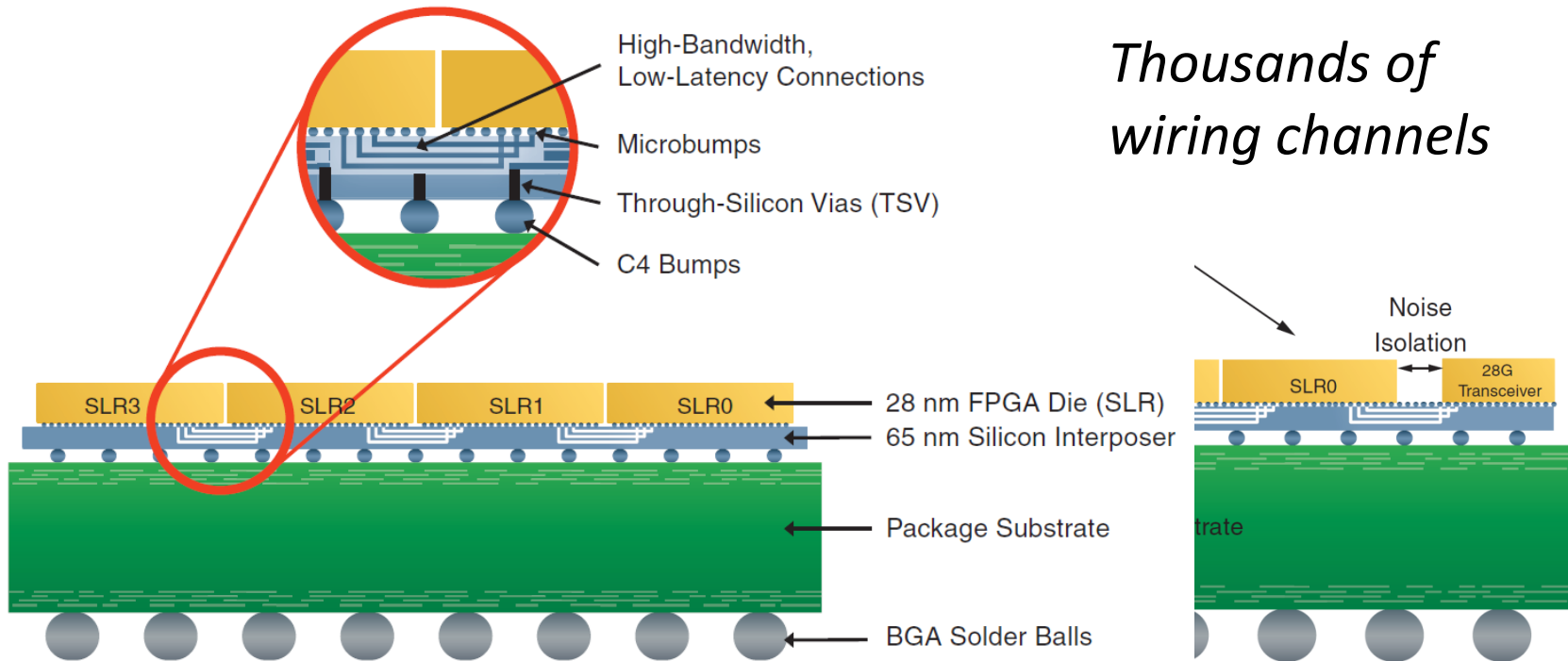
Thousands of wiring channels

High-Bandwidth, Low-Latency Connections

Microbumps

Through-Silicon Vias (TSV)

C4 Bumps

Noise Isolation

SLR3   SLR2   SLR1   SLR0   — 28 nm FPGA Die (SLR)

— 65 nm Silicon Interposer

SLR0   28G Transceiver

Package Substrate

BGA Solder Balls

Xilinx white paper #380 pg 4 & 7, 2012: Stacked Silicon Interconnect Technology

HLS (High Level Synthesis)

"Work in Progress"

- 1980s VHDL & Verilog RTL
    (Register Transfer Language)
- 2004 C, C++ or SystemC to VHDL/Verilog
    Matlab to VHDL/Verilog
- 2011 Xilinx bought AutoESL, incorporated HLS technology into their Vivado tool.
- 2011 OpenCL for uP, DSP, GPU & FPGAs
- Uses: Productivity
    FPGA development by software engineers

Floating-point

- 2015   32-bit Add/subtract/multiply
  Altera Arria-10 & Stratix-10

- IEEE floating-point library: exponent & mantissa size bit adjustable

- Uses:

  Super computer applications

  Wide dynamic range DSP

2019 High End Processing

- High performance PC: x86, 64-bit ARM, etc
- DSP: the niche is evaporating/morphing
- ASICs: high NRE
- GPGPU (General Purpose Graphics Proc. Unit)
  - Originally for gaming, **now used for AI apps**
- FPGAs (Field Programmable Gate Arrays)
  - As chip capacity increases, capabilities escalate

2019 Xilinx ACAP: Adaptive Compute Acceleration Platform

- https://www.eejournal.com/article/xilinx-previews-next-generation/

- HW/SW programmable engines
  - Probably enhanced DSP modules
    https://www.youtube.com/watch?v=XMeKwtI82M8

- Application and Real-Time Processors
  - Probably ARM or RISC-V uP

- On-die network fabric
  - See Jan Gray's http://fpga.org/grvi-phalanx/

2019 Intel/Altera:

- Singularity Prosperity series of videos:

  https://singularityprosperity.com/videos

  The Future of Classical Computing (Heterogeneous Architecture – CPUs, GPUs, FPGAs, ASICs,...):

  https://www.youtube.com/watch=2yklU69Xiuo

  The GPGPU (nVidia) argument:

  https://www.youtube.com/watch?v=658n_Ym8dkk

- Intel has many irons in the fire, along with Microsoft, Google, ...

  https://www.nextplatform.com/2018/05/24/a-peek-inside-that-intel-xeon-fpga-hybrid-chip/

References

- *Three Ages of FPGAs: A Retrospective…*, Steve Trimberger, Proc. IEEE v103#3p318, 2015

  www.cpe.virginia.edu/grads/pdfs/January%202016/VLSI.pdf

  forums.xilinx.com/t5/Xcell-Daily-Blog/Video-The-Three-Ages-of-the-FPGA-and-the-Age-of-the-Design/ba-p/644396

- *Xilinx Part Family History*, John Lazzaro,

  www-inst.eecs.berkeley.edu/~cs294-59/fa10/resources/Xilinx-history/Xilinx-history.html

- *Altera History*, corporate,

  www.altera.com/about/company/history.html

- HLS (High Level Synthesis)

  en.wikipedia.org/wiki/High-level_synthesis

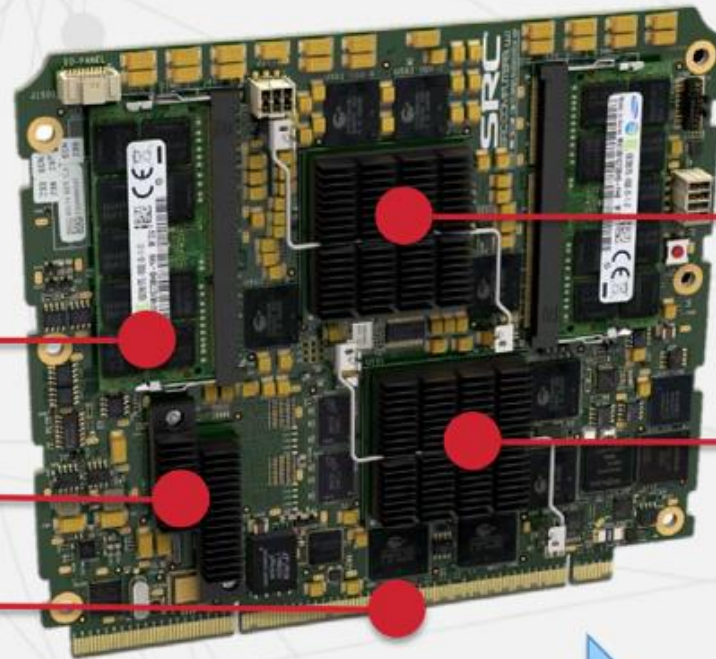# High End Applications

Typical FPGA & uP module

SRC Saturn 1 Server

64GB SDRAM (Two Banks)

Intel Microprocessor

Multiple GigE Ports

Use...

Syste...

42 Saturn 1 Servers per 4U chassis~2,000 watts
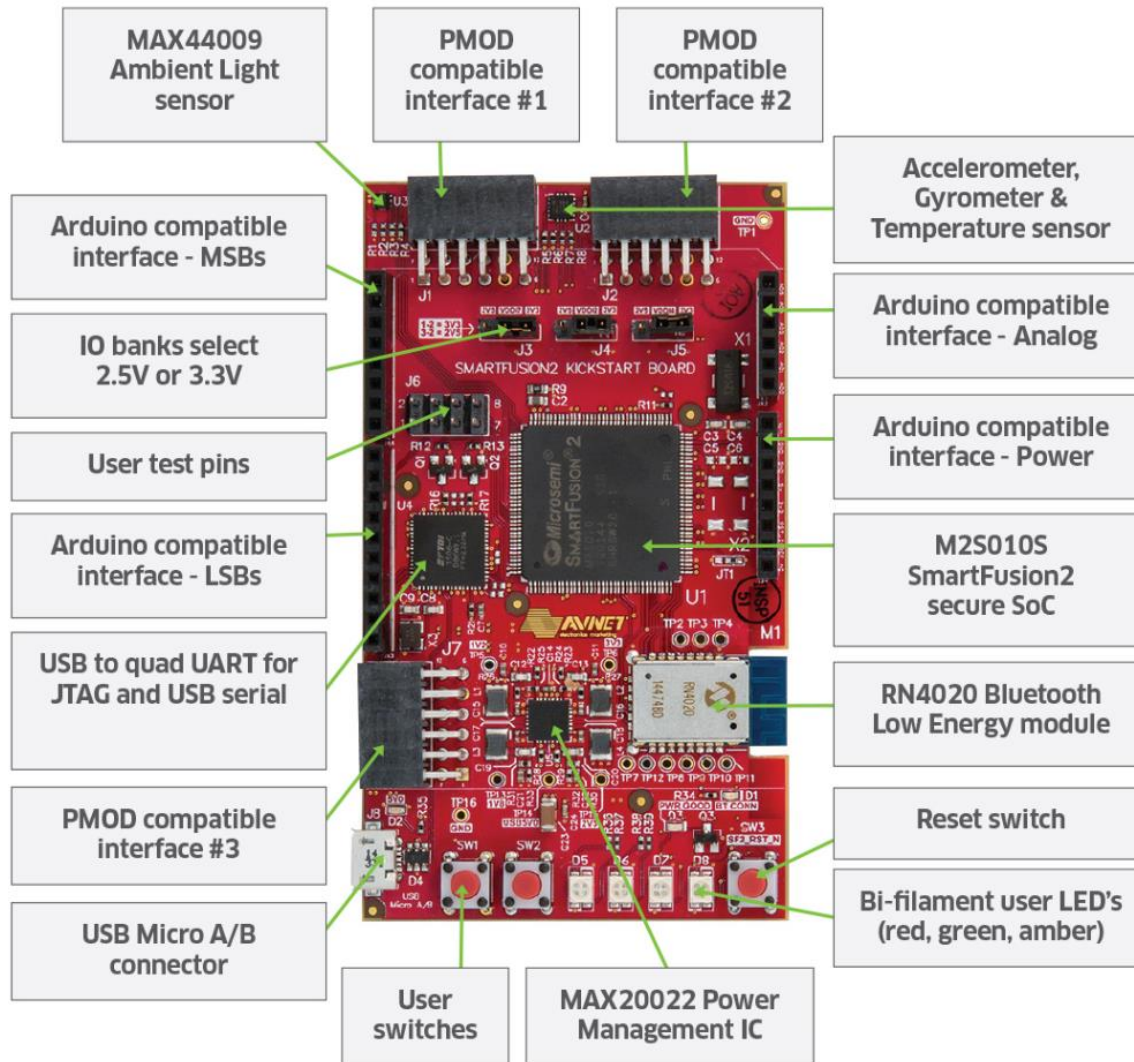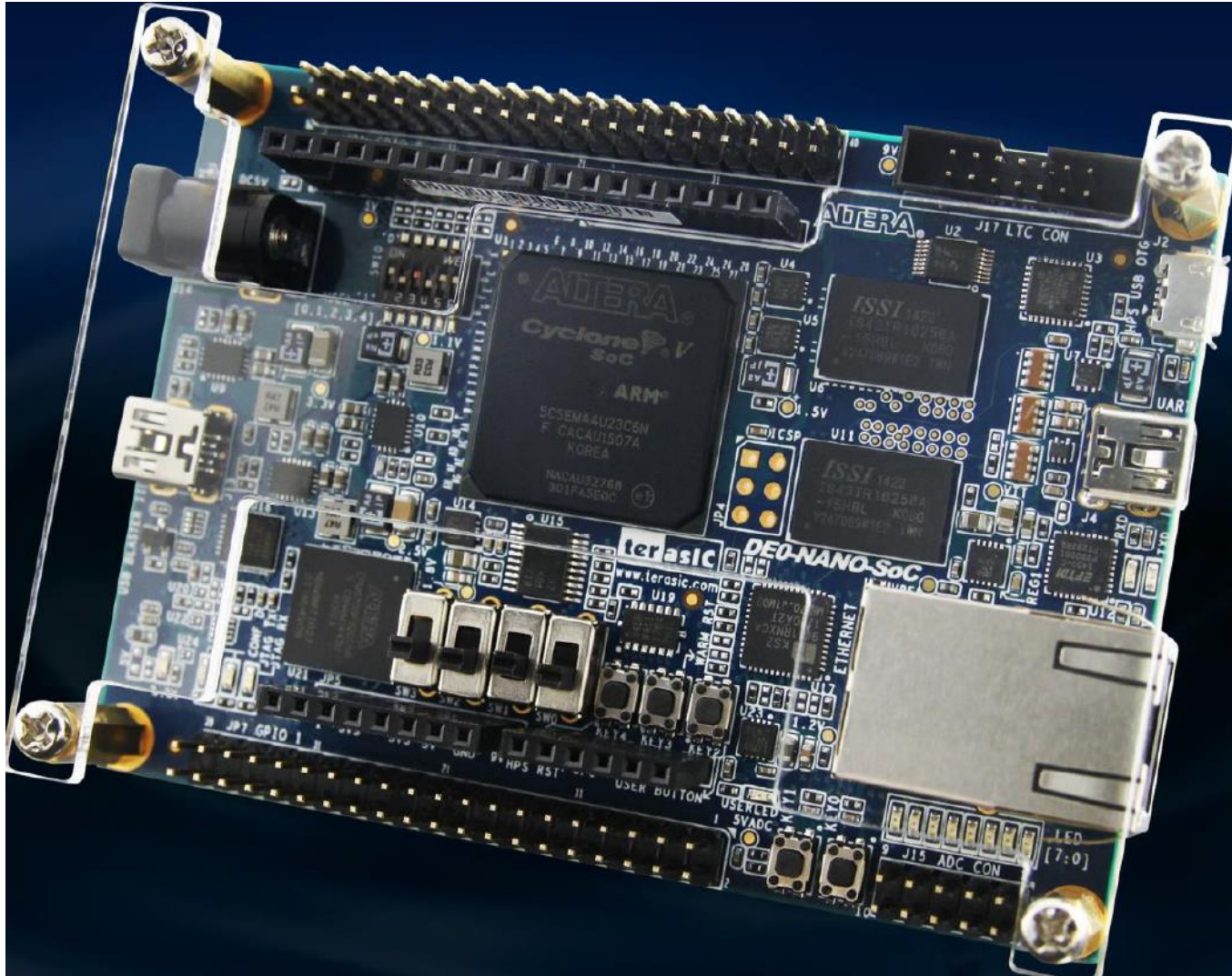
9 chassis per rack ~20,000 watts

High End Applications

ALDEC HES-7
Board using
(6) Virtex-7 2000
with 1.1M LUTs
each
Used to simulate
600M ASIC gates

Actel SmartFusion2 KickStart Kit

MAX44009 Ambient Light sensor

PMOD compatible interface #1

PMOD compatible interface #2

Arduino compatible interface - MSBs

IO banks select 2.5V or 3.3V

User test pins

Arduino compatible interface - LSBs

USB to quad UART for JTAG and USB serial

PMOD compatible interface #3

USB Micro A/B connector

User switches

MAX20022 Power Management IC

Accelerometer, Gyrometer & Temperature sensor

Arduino compatible interface - Analog

Arduino compatible interface - Power

M2S010S SmartFusion2 secure SoC

RN4020 Bluetooth Low Energy module

Reset switch

Bi-filament user LED's (red, green, amber)

Avnet
AES-SF2-KSB-G
$59.95
Has ARM
 Cortex M3

Xilinx Zynq SOC kit
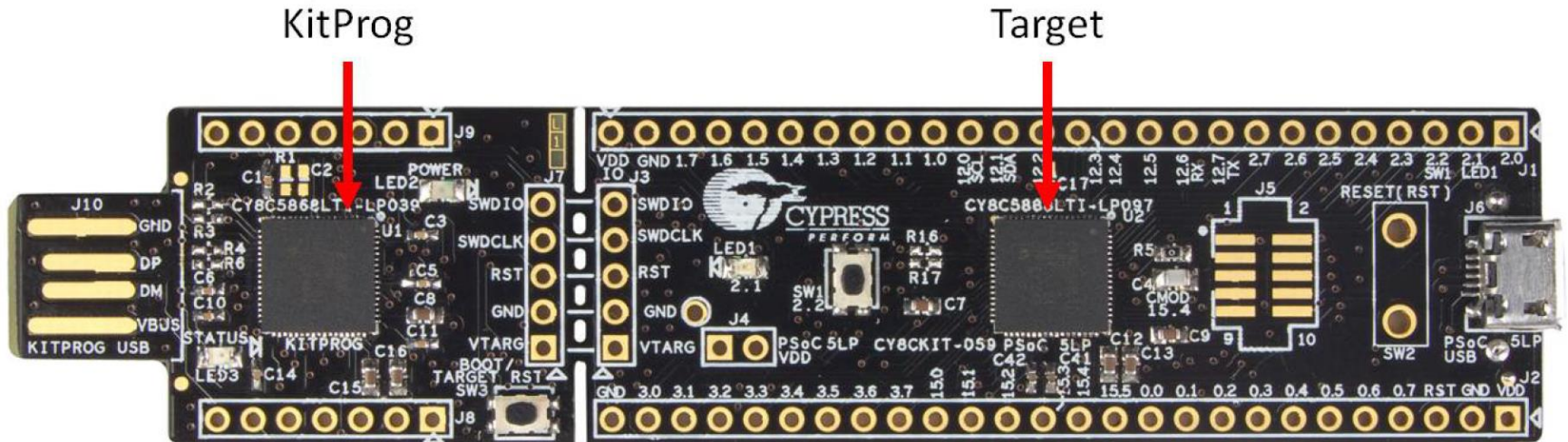
Snickerdoodle with WiFi & Bluetooth $72

Altera Cyclone V SOC kit

Terasic
DE-0
Nano SoC
$99

Cypress PSoC5 kit

CY8CKIT-059 for $10 with: ARM Cortex M3, Analog & Digital IO

IP (Intellectual Property)
Pre-packaged modules, macros & generators

- TTL logic equivalents (with schematic entry)
- Simple macros (also with schematic entry)
- Vendor free IP: soft-core processors, CORDIC, FFT, Floating-point, PCI-express, memory controllers …
- Open source IP: www.opencores.org
- Vendor and 3rd party non-free IP (various interfaces, soft core processors, image processing…)
- Uses: save time & money

Xilinx CORDIC GUI

Ray Andraka 1998: A survey of CORDIC algorithms for FPGA based computers
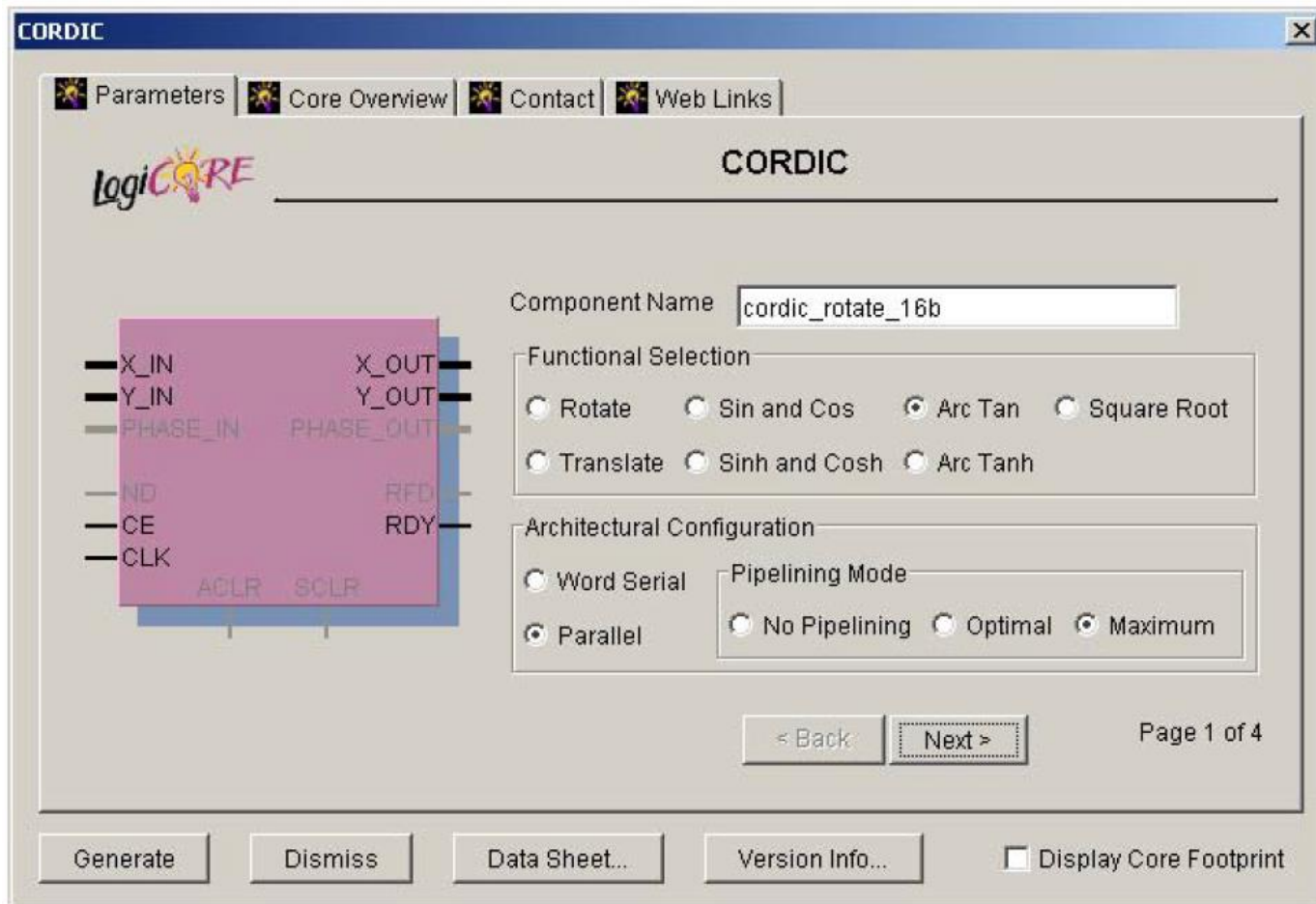
Intro: Experience

- PowerPC emulation of Pentium
  - Decided to learn VHDL   1995
- AMD/Vantis/Lattice Semi
  - Competitive benchmarking   1998-2002
- OnBoard Software/BAE Systems   2004-2012
  - FLR-9, IP over 1553, Weather RADAR
- ROIS24_24uP
  - 24-bit soft core processor   2016

FPGA Code & Test Process

- Schematic capture (doesn't scale)
- Or write RTL (Register Transfer Logic) which evolved into Verilog and VHDL (1980s)
- Simulate
  - Faster than compile/map-pack-P&R-bit-stream/download
  - Use test-bench
  - Not perfect
- Compile: synthesize VHDL/Verilog to gates or FPGA primitives
- Map, Pack, timing driven Place & Route
- Bit-stream generation
- Download & test